IONQ

Chip-Scale Technology Development for Trapped-Ion Quantum Computer Systems

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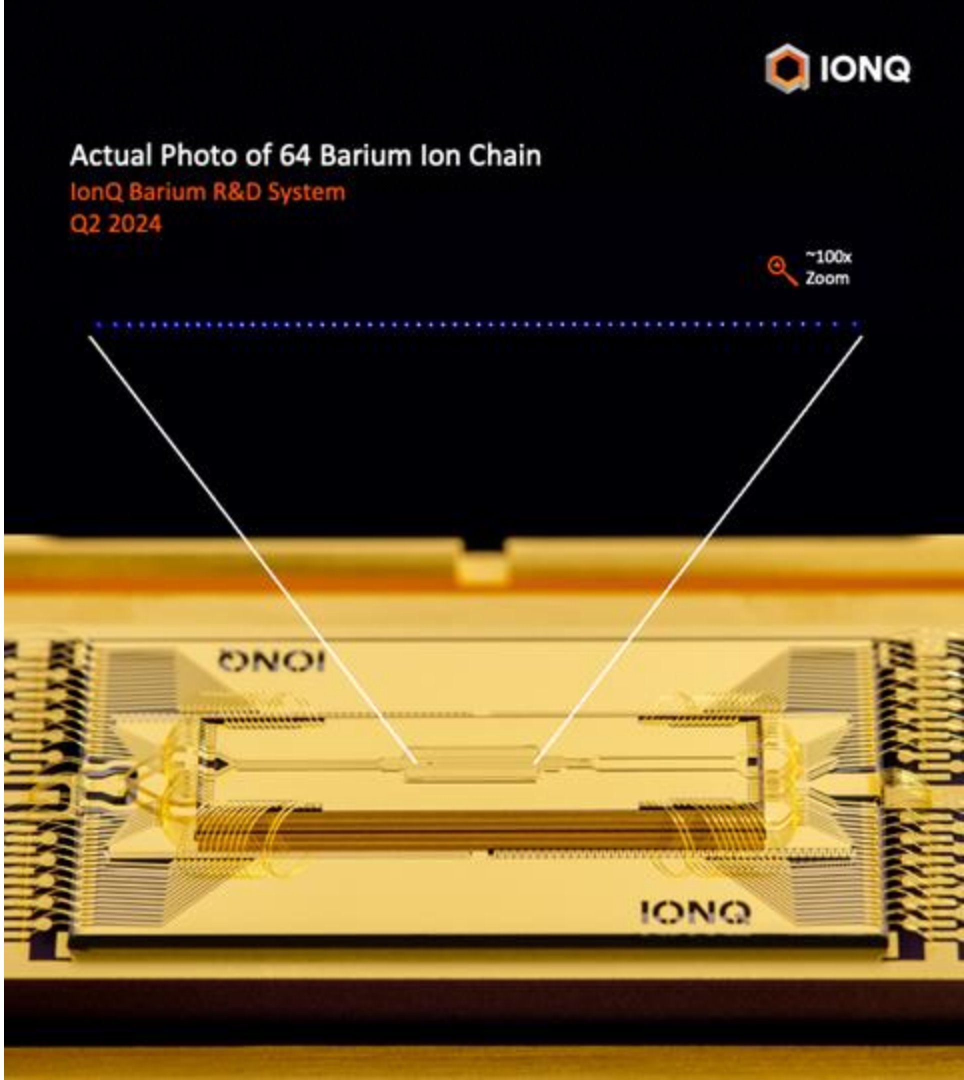
IonQ's mission:

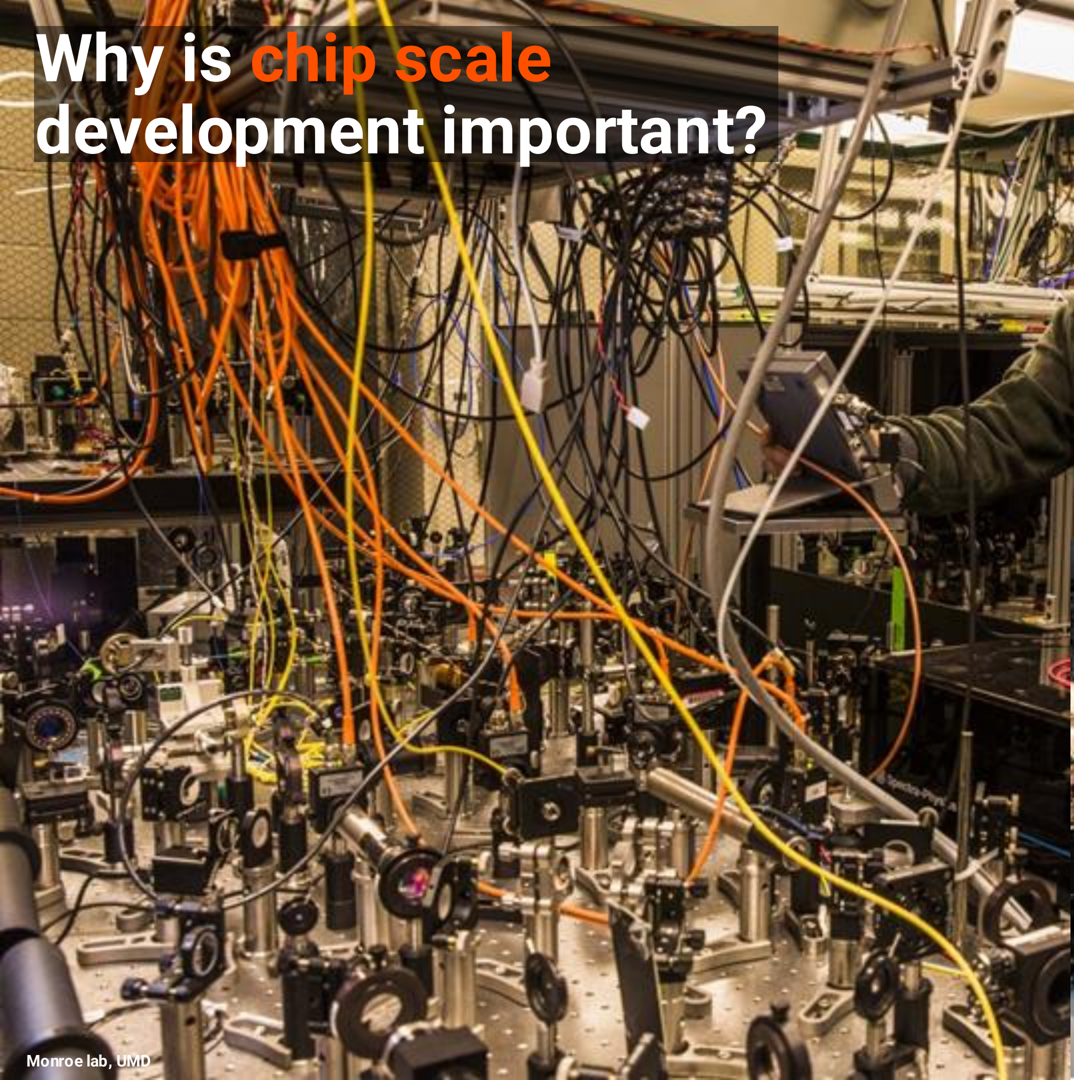
To build the world's best quantum computers to solve the world's most complex problems.

Individual atomic ion qubits in an ion trap have many superior properties to competing modalities.

- Identical and naturally quantum
- Long coherence and qubit lifetime
- Unparalleled inherent performance
- Reconfigurable and highly connected
- Modular and scalable system architecture
- Capable of running at room temperature
- Naturally photonically active



Why is chip scale development important?

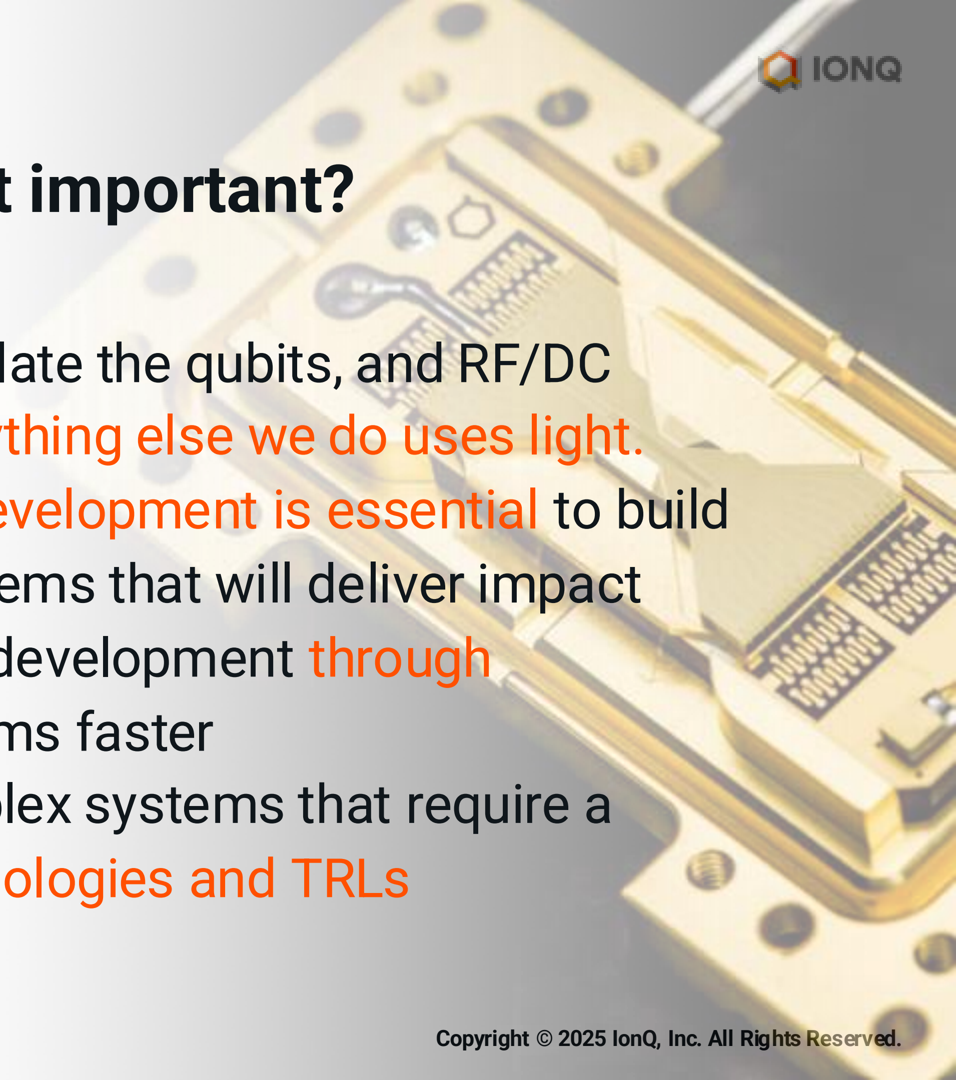


Monroe lab, UMD

This is state of the art for academic labs, and it is where IonQ started almost 10 years ago.

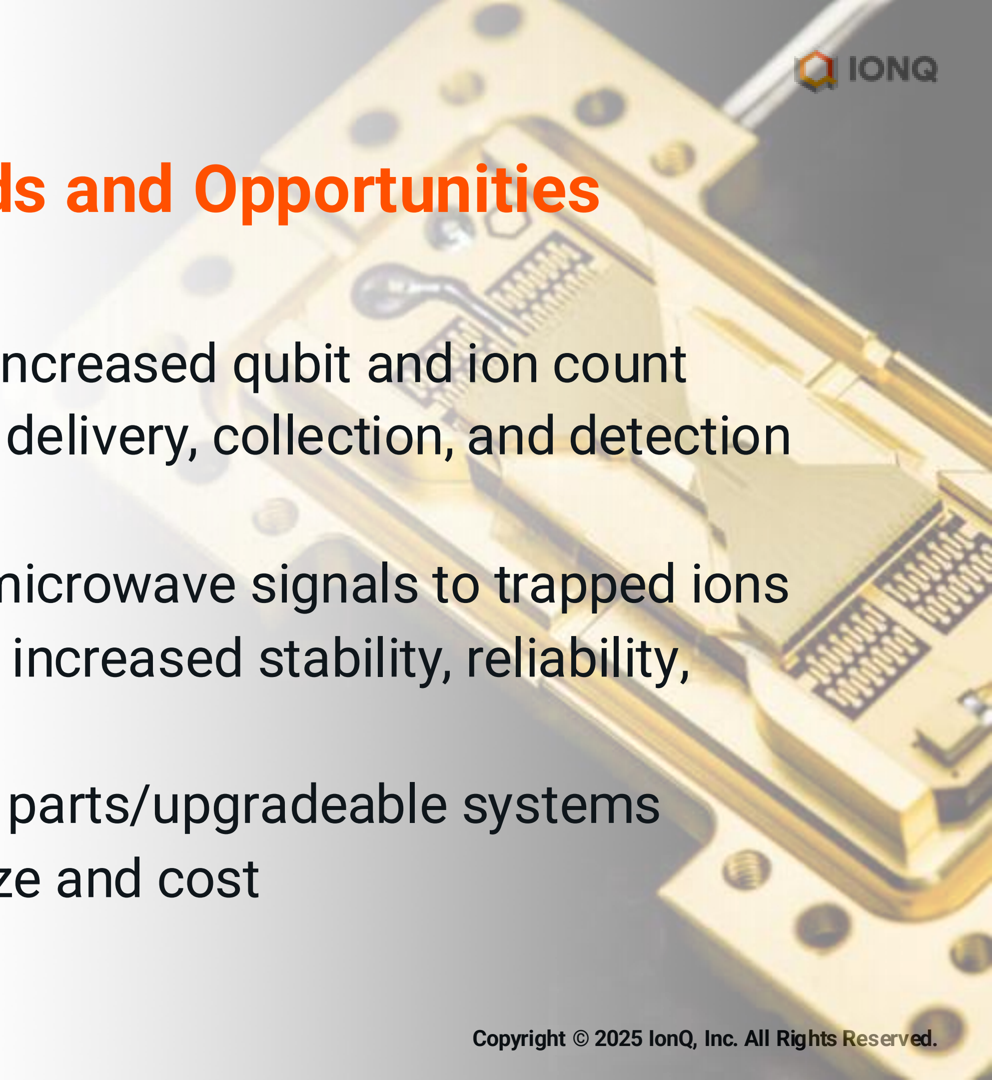
Blatt lab, Innsbruck

Why is chip scale development important?



Summary

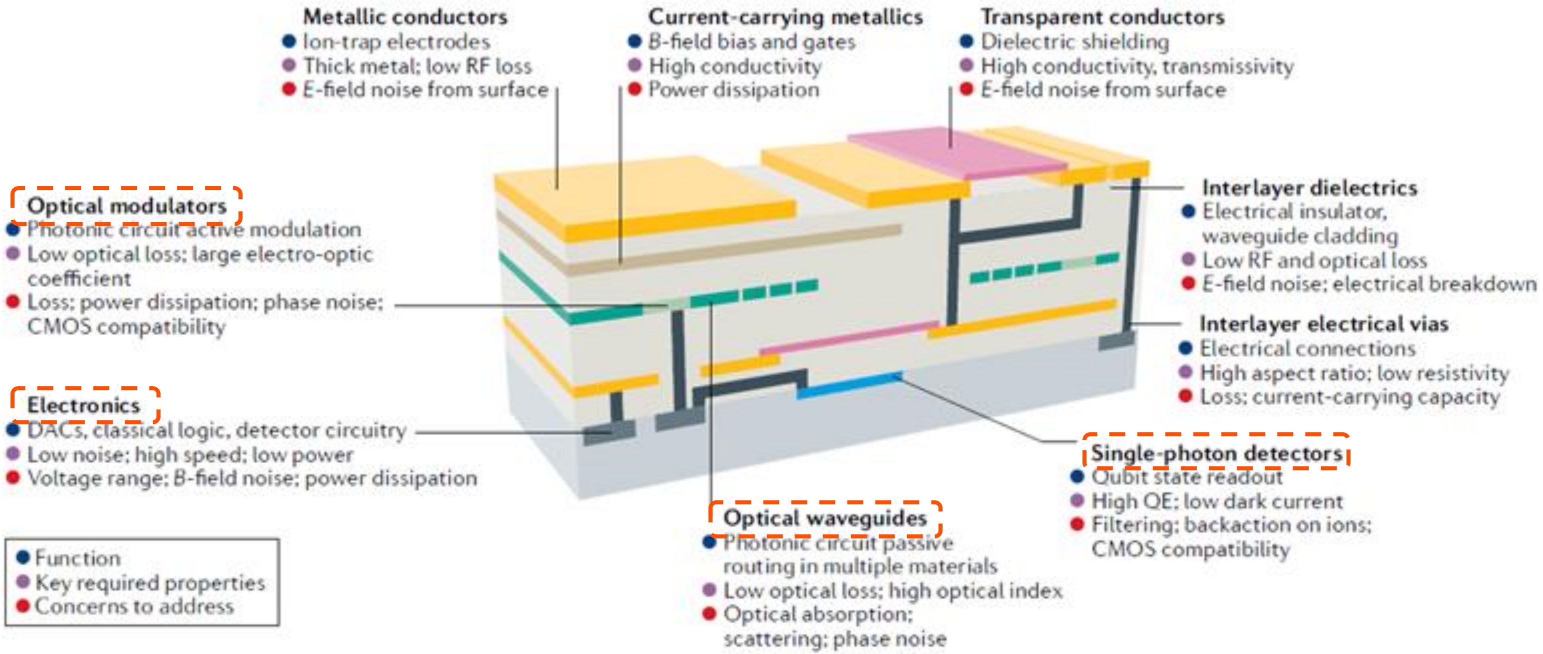
- We use vacuum and shielding to isolate the qubits, and RF/DC fields to hold and shape them. Everything else we do uses light.
- Successful chip-scale technology development is essential to build trapped-ion quantum computer systems that will deliver impact
- We need to find ways to accelerate development through collaborations to get to better systems faster
    - Quantum computers are complex systems that require a wide range of chip-scale technologies and TRLs



Chip-Scale Technology: Needs and Opportunities for Industry and Systems

- Scalable ion trap technology for increased qubit and ion count
- Scalable generation, modulation, delivery, collection, and detection of visible to NIR light
- Scalable delivery of DC, RF, and microwave signals to trapped ions
- Performance improvements with increased stability, reliability, manufacturability, and up-time
- Modularity to enable replaceable parts/upgradeable systems
- Reduction of quantum system size and cost

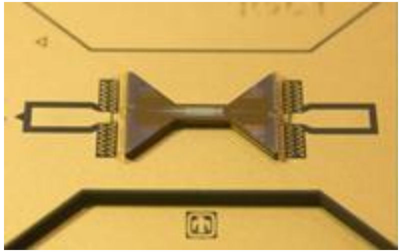
Devices for Trapped-Ion QC: Monolithic Integration



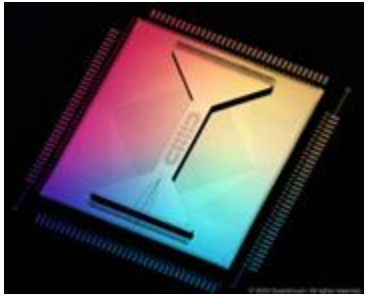
K. Brown, et al. *Nature Reviews Materials* **6**, 892–905 (2021)

State of the Art: Ion Traps

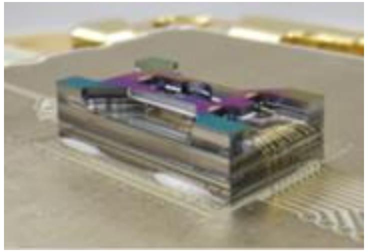
Sandia NL: Peregrine Trap



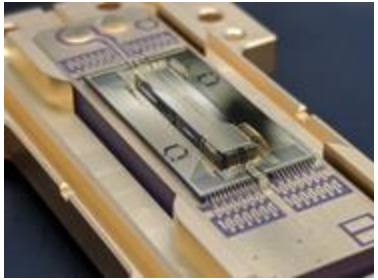
Quantinuum: H2 Trap



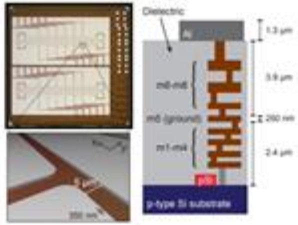
Infineon: Gen3 Trap



IonQ: MGT



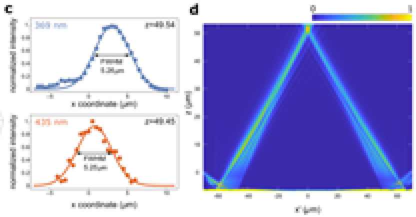
MIT-LL/MIT: “CMOS” Trap



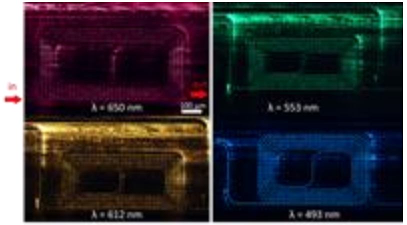
- Multi-layer surface electrode ion traps
  - Wafer-scale microfabrication
  - High-precision features
  - Small form factor
  - High-density and complex signal routing
  - Platform for further integration
  - “3D” traps may offer some advantages
- QC-focused ion traps have begun to move from the lab (research) to fab (industry)
  - Yet still no agreed-upon standard technology platform
  - Differing system needs?

State of the Art: Visible Photonics - Passives

Sandia NL: SiN, Alumina

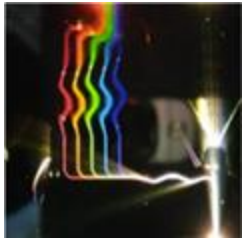


IonQ: SiN



MIT-LL: SiN, Alumina

LioniX: SiN, Alumina

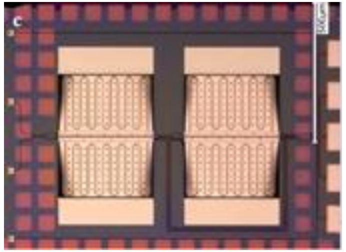


- Other Development Efforts
  - ETH, Max Planck, IMEC, AIM, AMF, MIT, AFRL, Columbia, Cornell, NIST, UCSB, Tufts (SiN)
  - AlUVia, Yale (Alumina)

- Multi-layer passive PICs for routing and delivery of visible light to and from free-space
  - Single-mode PM waveguides
  - Vertical grating couplers
  - Edge couplers
  - On-chip splitters
  - Monolithic integration into ion traps
- Some small foundries offer visible PIC tech platforms, MPWs
  - Primarily SiN, though Alumina is becoming available
  - No PDKs yet - wavelength range is large!
  - Not many fabs can do both PICs and MEMS-style ion trap tech

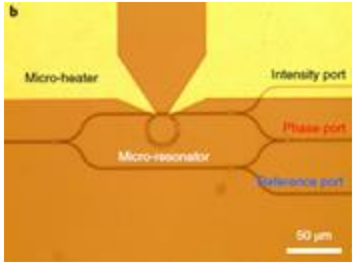
State of the Art: Visible Photonics - Modulators

Sandia NL: AlN/SiN MEMS

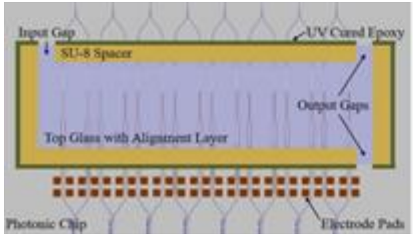


Hyperlight/Harvard: TFLN EO

Columbia University: SiN Thermal



MIT: SiN/Liquid Crystal



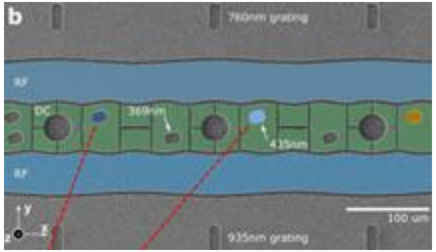
Other Development Efforts

- Yale, MIT, AFRL, AIM: AlN EO

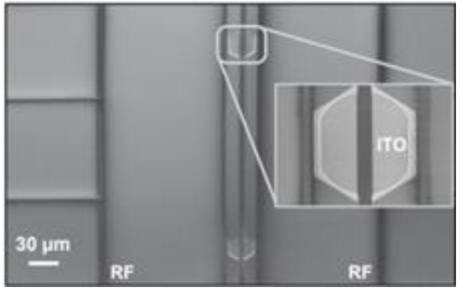
- Visible light modulators
  - Scalable active control of amplitude, frequency, and phase of light to ions
  - Enables dynamic routing of light
- Technology mostly still low TRL (1-3)
  - No agreed-upon standard technology platform
  - Device length scale (mm) often not considerably smaller than bulk modulators
  - Different use cases for different tech?

State of the Art: Integrated Single-Photon Detectors

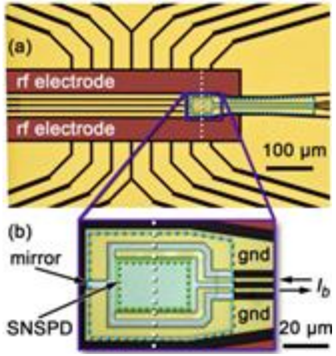
Sandia NL: Trap-integrated Si SPAD



MIT-LL: Trap-integrated Si SPAD



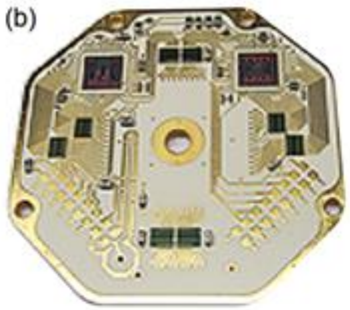
NIST Boulder: Trap-integrated NbTiN SPAD



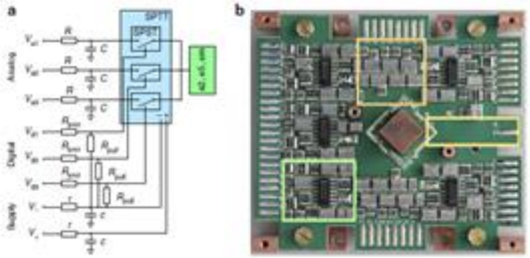
- Generally, chip-scale single-photon detector technology is high TRL and well-matched to trapped-ion QC needs
  - APDs
  - SNSPDs
- Monolithic integration into ion traps demonstrated by multiple research groups
- Questions of integration such as light scatter and noise

State of the Art: Integrated Electronics

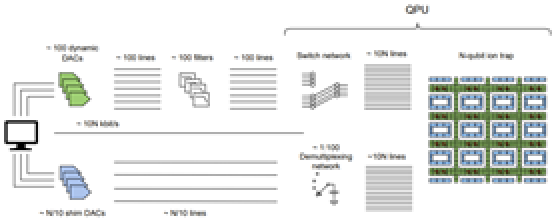
GTRI: DACs- hybrid integration with trap



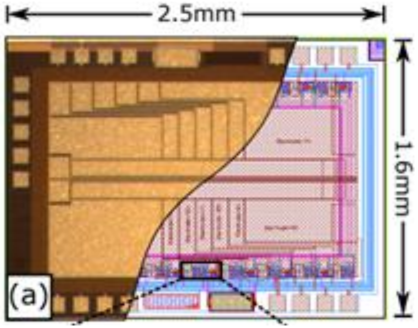
ETH Zurich: Switches- hybrid integration with trap



Oxford Ionics: "WISE" Switch-based architecture



MIT-LL: DACs- monolithic integration with trap



- Commercial and custom DAC and switch ICs integrated with ion traps for "DC" trap voltages
  - Leverages high-TRL IC technology
- No integrated RF/microwave electronics yet (except for microwave transmission lines)
- Different voltage generation/delivery

Chip-Scale Technology: Challenges for Industry

Technical Performance Challenges: Device performance, co-integrability, proximity to sensitive qubits

- Quantum computers require exquisite device performance
  - While some integration approaches will improve performance (e.g., optical stability from PICs), there is little room for tradeoffs between performance and scalability/SWAP-C
  - This also applies to co-integrability of different devices and compatibility of required materials
- Required system environment can be restrictive (e.g., UHV, cryo)
- Still many known and unknown unknowns!

Chip-Scale Technology: Challenges for Industry

Tech-Development Challenges: Increasing TRL at required pace with successful offramps for system integration

- Chip-scale technology development is expensive and long microfabrication run times set the development timescale
  - For simultaneous monolithic integration of multiple technologies, costs and run times may be prohibitive
- Commercial microfabs/foundries have the tools but not the processes for trapped-ion QC tech needs
- TRL is not well-defined without integrated system requirements
  - How do you know if what you are making is good enough for the (future) system?

Chip-Scale Technology: Challenges for Industry

Organizational Challenges: Effective external collaborations, foundry models, synergistic non-quantum applications

- Quantum-chip volume demands (i.e. low) are a poor fit for commercial microfabs
    - Likely will remain true even as systems scale, but particularly problematic for early-stage development and low-volume system production
    - There are few (if any) other big industries that have similar chip-tech needs to trapped-ion QC
- For the quantum industry, it can be cost, time, and "workforce"-prohibitive to be vertically integrated and build/operate microfabs
    - The quantum workforce is limited and spread thin across institutions, qubit modalities, and even within modalities
    - We're seeing the start of the expanded quantum education (non-physics and non-PhD) programs and industry workforce training

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Are you convinced chip scale development important?

Conclusion

- Chip-scale technology is essential for trapped-ion quantum computer systems to scale in qubit count, system performance, SWAP-C, and manufacturing.
- There is excellent, ongoing development at IonQ and within the community, but now is the time to accelerate development through collaborations!
- There has been great progress so far, but more is needed! There exist challenges around component performance, integrated system development, and organizational alignment.
- IonQ is looking to partner and collaborate! hudek@ionq.co

Thank you.